

ABSTRACT OF THE DISCLOSURE

An object of the present invention is to make it possible to effect a reliable and compact configuration for a semiconductor device when mounting a plurality of 5 semiconductor elements in a single package, and achieve higher integration and higher functionality more effectively. In a multi-layer wiring board 20 in which wiring patterns (conductor layers) 22, 24, and 26, and insulating layers 23, 25, and 27, are formed alternately in multiple layers on a 10 base substrate, and electrically connections are made between the wiring patterns through via holes VH1 and VH2, semiconductor elements 30 are imbedded and mounted inside the insulating layers 23, 25, and 27, and the semiconductor elements 30 are deployed so that they are electrically 15 connected to wiring patterns that are covered by the insulating layers, and so that they are stacked up in a direction perpendicular to the planar dimension of the multi-layer wiring board 20.

PROPRIETARY MATERIAL  
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